UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,944	08/31/2000	Oleg Drapkin	ATI-000152BT	3407

25310 7590 04/08/2002

VOLPE AND KOENIG, PC
DEPT ATI
SUITE 400, ONE PENN CENTER
1617 JOHN F KENNEDY BLVD
PHILADELPHIA, PA 19103

EXAMINER	
NGUYEN, HIEP	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/651,944	Applicant(s) DRAPKIN ET AL.	
	Examiner Hiep Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 11-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 11-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitations "a first circuit", a second circuit", "a control circuit" in claims 14, 16 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 2 and 11 are objected to because of the following informalities: the recitation "an said circuit " in claim 2 should be changed to --said circuit--. The recitation "comprising the step of" in claim 11 should be changed to -- comprising--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 14-17 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claim 14, the recitation "a first circuit element for selectively providing current to said parasitic capacitance" is indefinite because it is misdescriptive. According to figure 2C of the present application, the first element (assumed to be 20) provides current to the parasitic capacitance (Cp) but there is no control seen on element (20) i.e., no selection. Thus the "a first circuit element" does not selectively provide current to the parasitic capacitance. The

recitation "a second circuit element for... into said input" is indefinite because it is unclear what is the input of the circuit. Assume that the input of the circuit is pad (P) then the parasitic capacitance (Cp) is "coupled" directly to the input. Thus there is no mean to prevent the parasitic capacitor to discharge directly into "said input". Applicant is respectfully requested to point out what is the "a second circuit". The recitation " a control circuit monitoring said input signal... when a negative going edge of said input signal is detected" is indefinite because it is unclear which drawing shows the "a control circuit". The same analysis is true for claim 16,

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-6, 8, 9, 11-15 and 18-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishikawa et al. (Japanese Pat. JP02000252430A).

Regarding claims 1 and 2, figure 1 of Ishikawa shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance, comprising the steps of:

detecting a direction of change of the input voltage at input (1);

introducing a current to the parasitic capacitance (3) via buffer (6) at the positive edge of the input signal to charge the parasitic capacitance (4) for compensating the current of the input signal. Note that figure 2 does the same function. In figure 2, the current introducing to the parasitic capacitor is supplied by (5) when a rising edge of the input signal is detected.

Regarding claims 3 and 19, the output of (6) always has a voltage equivalent to the input voltage. Thus, capacitor (3) does not conduct any current and the parasitic capacitor (4) cannot discharge into the input of the circuit. Thus, discharging of parasitic capacitance (4) into the input signal is prevented. The parasitic capacitance (4) is across the input (1) and ground. Element (6) introduces a current to the input.

Regarding claims 4, similar to the method of claim 1, the impedance of the parallel circuit (5) change when transistor (2) is turned on in response to a positive edge of the input signal to reduce distortion of the input signal.

Regarding claim 5, figure 2 of Ishikawa shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a detection circuit (6) for detecting changes of the input voltage; a correction circuit (5) coupled to the detection circuit will be activated for compensating the current from the input signal diverted to the parasitic capacitance due to the positive edge of the input signal.

Regarding claim 6, the detection circuit (6) inherently includes a capacitance (gate-source capacitance).

Regarding claim 8, figure 1 of Ishikawa shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a detection circuit (2) for detecting the change of the input signal and a correction circuit (6) for compensating for current from the parasitic capacitance (4) to be added to the input signal due to a negative edge of the input signal. Note that when the input signal is at negative edge, the output of element (6) is at low level. Thus, the parasitic capacitance (4) is discharged through element (6) to compensate the current from said parasitic capacitance.

Regarding claim 9, the detection circuit includes capacitance (3).

Regarding claim 11, figure 1 shows a detecting circuit (6) and a correction circuit (2) for changing the impedance of a parallel termination circuit (5) that is in parallel with the parasitic capacitance (4).

Regarding claim 12, the claim circuit is identical to the circuit of claim 1 and it is read in figures 1 or 2 of Ishikawa.

Regarding claim 13, the claim circuit is identical to the circuit of claim 3 and it is read in figures 1 or 2 of Ishikawa.

Regarding claim 14, figure 2 (or figure 1) of Ishikawa shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a first element (5) for providing current to the parasitic capacitance, a second circuit element (3) blocking the discharge of the parasitic capacitance and a control circuit (2). Note that the second circuit element (3) is "turned off" (isolated) when a positive

voltage from the control circuit (2) applies to its negative terminal and circuit (3); it is "turned on" when circuit (2) does not conducts due to a negative going edge input signal is applied to the input (1).

Regarding claim 15, first and second circuit elements (5, 3) have a common terminal coupled to the parasitic capacitor (4).

Regarding claim 18, the parasitic capacitance (4) is across the input (1) and ground.

Regarding claim 20, the parasitic capacitance (4) appears between the input (1) and ground.

Regarding claim 21, the parasitic capacitance (4) appears between the input (1) and ground.

Regarding claim 22, the parasitic capacitance (4) appears between the input (1) and ground.

Regarding claim 23, the parasitic capacitance (4) appears between the input (1) and ground. Element (6) introduces a current to the input.

Regarding claim 24, the parasitic capacitance (4) appears between the input (1) and ground.

Regarding claim 25, the detection circuit (2) inherently has a capacitance (gate-source or gate-drain capacitance) that is connected to one terminal of the parasitic capacitance (4).

Regarding claim 26, figure 2 show a method for reducing distortion of a signal applied to the input of a circuit having c parasitic capacitance, comprising the steps of:

detecting a direction of change in voltage of said input signal (element 6)

introducing a current to the parasitic capacitance (element 6) responsive to detection of a positive edge of the input signal, thereby eliminating a need for an additional parasitic capacitance to reduce distortion.

Regarding claim 27, when the "negative edge" is detected, the parasitic capacitance (4) cannot discharge into the input because the potential of the two terminals of (3) is always equal.

Response to Arguments

In the remarks Applicant argues that the Japanese reference (430) needs two parasitic capacitors (3) and (4) to function and the present application requires only one parasitic capacitor. The parasitic capacitance is a "by-product" of an electrical element. In a monolithic integrated circuit, the capacitors and diodes are formed between the planned circuit elements and the substrate during processing. They are parasitic elements. The parasitic capacitor (Cp) in figure 2C of the present application and the combination of parasitic capacitors (3) and (4) are

basically similar. (Cp) is the combination of the capacitances formed by the gate and the source or by the gate and the drain of transistor (14) combined with the capacitance formed by the PAD, the connecting wire and the substrate. Similarly, (3) and (4) are ones of the parasitic capacitances (associated with the) at the input (1) of the circuit. Figures 1 or 2 of reference (430) shows that at the rising edge of the input signal, a current flows through the parasitic capacitor (4) and a current is introduced to the parasitic capacitance (4) via element (6) or (5) to compensate for "current of said input signal charging said parasitic capacitance responsive to detection of a positive edge of said input signal". As mentioned above, the combination of (3) and (4) is the parasitic capacitance at the input (1) of the circuit.

In figure 1 of reference (430), the detection circuit is buffer (6). In figure 2, the detection circuit is FET (2) because element (2) detects a rising edge of the input signal. At the rising edge of the input signal, (2) and (5) are turned on as a result, a current is introduced to the parasitic capacitor (2).

In page 7, 4th paragraph of the remark, the Applicant states that " It is submitted that there is no detection circuit for detecting **a change in parasitic capacitance** in the '488 patent". The parasitic capacitance of an element is fixed. Thus it is unclear how a parasitic capacitance can be changed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 746-5716. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
04-04-02

TUAN T. LAM
PRIMARY EXAMINER